



PSMN013-100YSF

9 July 2018

Objective data sheet

1. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	147	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 20\text{ A}; T_j = 25\text{ °C}$	-	9.9	12.3	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 20\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 10\text{ V}; \text{Fig. 5}$	-	4	-	nC
Source-drain diode						
Q_r	recovered charge	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	[tbd]	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	<p>LFPAK56; Power-SO8 (SOT669)</p>	<p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN013-100YSF	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

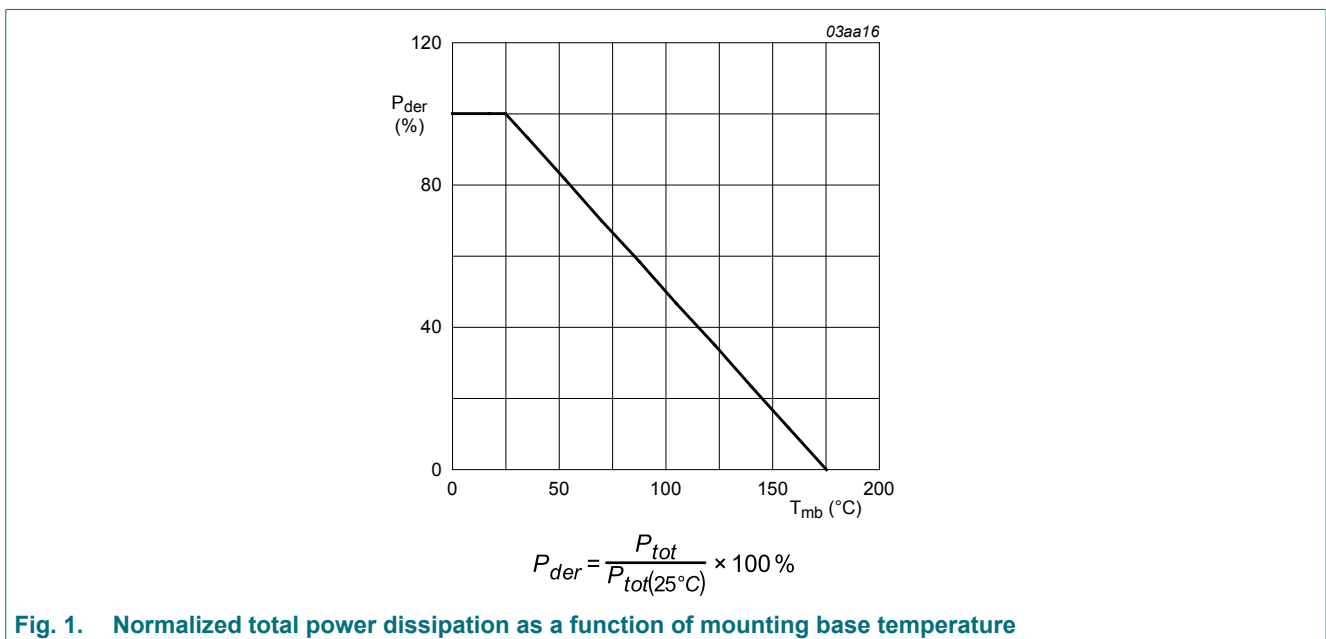
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	100	V	
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	100	V	
V_{GS}	gate-source voltage		-20	20	V	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	147	W	
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	-	75	A	
		$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}$	-	53	A	
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$	-	302	A	
T_{stg}	storage temperature		-55	175	°C	
T_j	junction temperature		-55	175	°C	
$T_{slid(M)}$	peak soldering temperature		-	260	°C	
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	-	75	A	
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$	-	302	A	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 25\text{ A}; V_{sup} \leq 100\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ Unclamped	[1]	-	158	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 100\text{ V}; V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ $R_{GS} = 50\text{ }\Omega$	[1]	-	25	A

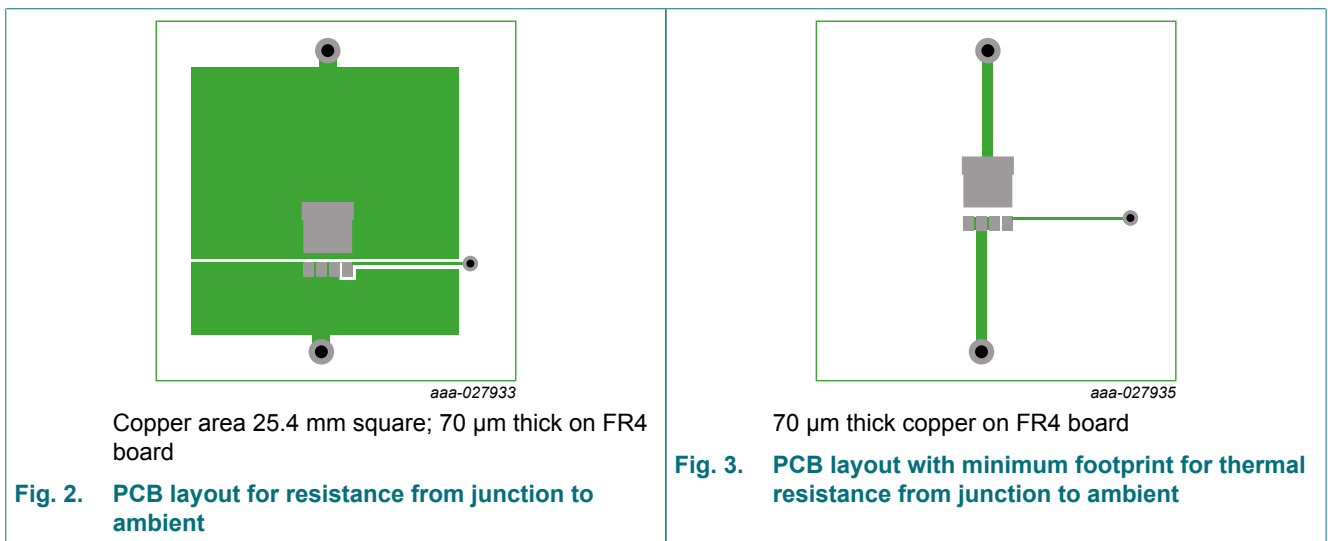
[1] Protected by 100% test



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	0.92	1.02	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 2	-	[tbd]	-	K/W
		Fig. 3	-	[tbd]	-	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.6	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.9	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{Fig. 4}$	2	3.1	4	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 175 \text{ }^\circ C$	-	-8	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	[tbd]	1	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	5	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	5	100	nA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 20 A; T _J = 25 °C	-	9.9	12.3	mΩ
		V _{GS} = 7 V; I _D = 15 A; T _J = 25 °C	-	12	17.5	mΩ
		V _{GS} = 10 V; I _D = 20 A; T _J = 100 °C	-	[tbd]	[tbd]	mΩ
		V _{GS} = 10 V; I _D = 20 A; T _J = 175 °C	-	[tbd]	25.8	mΩ
R _G	gate resistance	f = 1 MHz	-	2	-	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 20 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 5	-	31	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V	-	[tbd]	-	nC
Q _{GS}	gate-source charge	I _D = 20 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 5	-	8	-	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	[tbd]	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	[tbd]	-	nC
Q _{GD}	gate-drain charge		-	4	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 20 A; V _{DS} = 50 V; Fig. 5	-	[tbd]	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C	-	2034	-	pF
C _{oss}	output capacitance		-	454	-	pF
C _{rss}	reverse transfer capacitance		-	15	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2.5 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C	-	10.7	-	ns
t _r	rise time		-	9.3	-	ns
t _{d(off)}	turn-off delay time		-	17.4	-	ns
t _f	fall time		-	10	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 20 A; V _{GS} = 0 V; T _J = 25 °C	-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V	-	[tbd]	-	ns
Q _r	recovered charge		-	[tbd]	-	nC

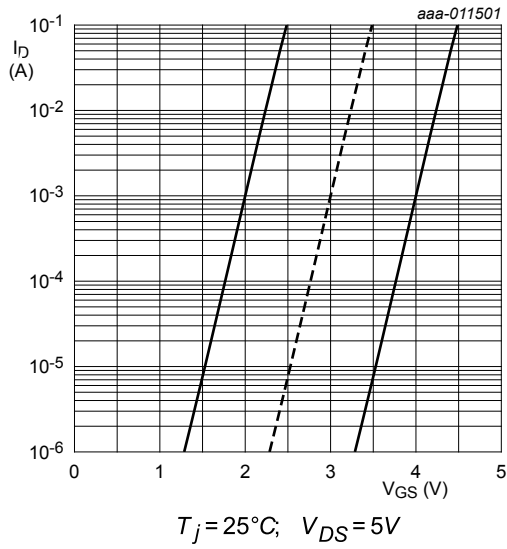


Fig. 4. Sub-threshold drain current as a function of gate-source voltage

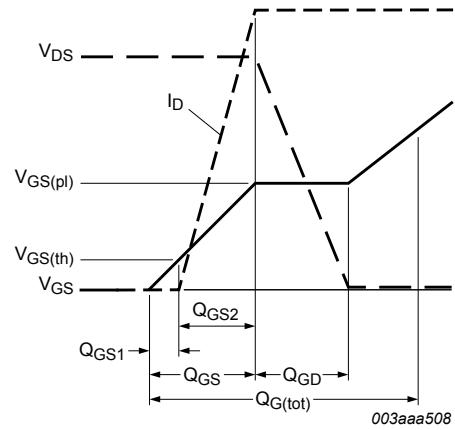
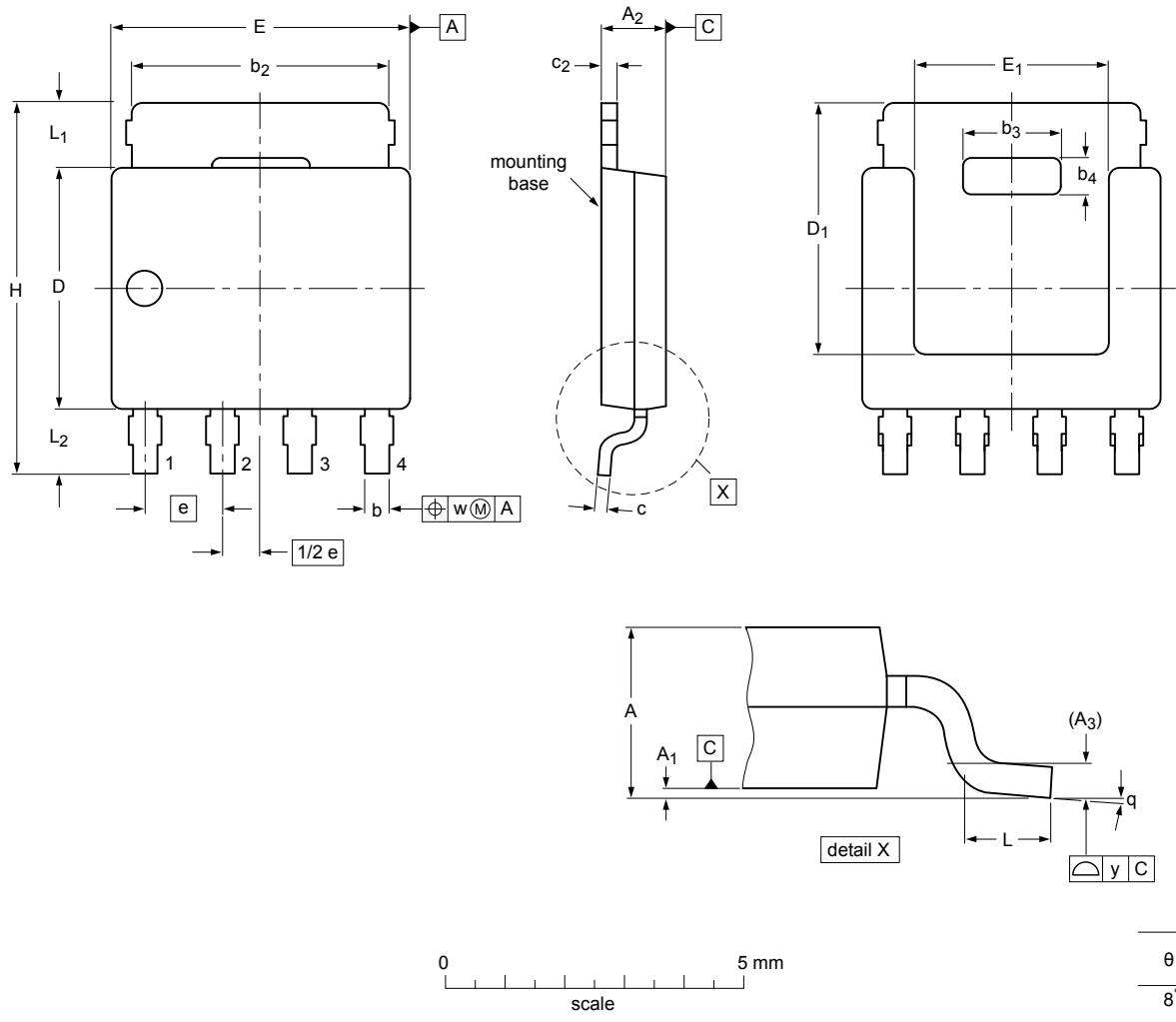


Fig. 5. Gate charge waveform definitions

7. Package outline

Plastic single-ended surface-mounted package (LFAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit ⁽¹⁾	A	A ₁	A ₂	A ₃	b	b ₂	b ₃	b ₄	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3	1.27	6.2	0.85	1.3	1.3		
nom				0.25																0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT669		MO-235			-11-03-25- 13-02-27

Fig. 6. Package outline LFAK56; Power-SO8 (SOT669)

8. Soldering

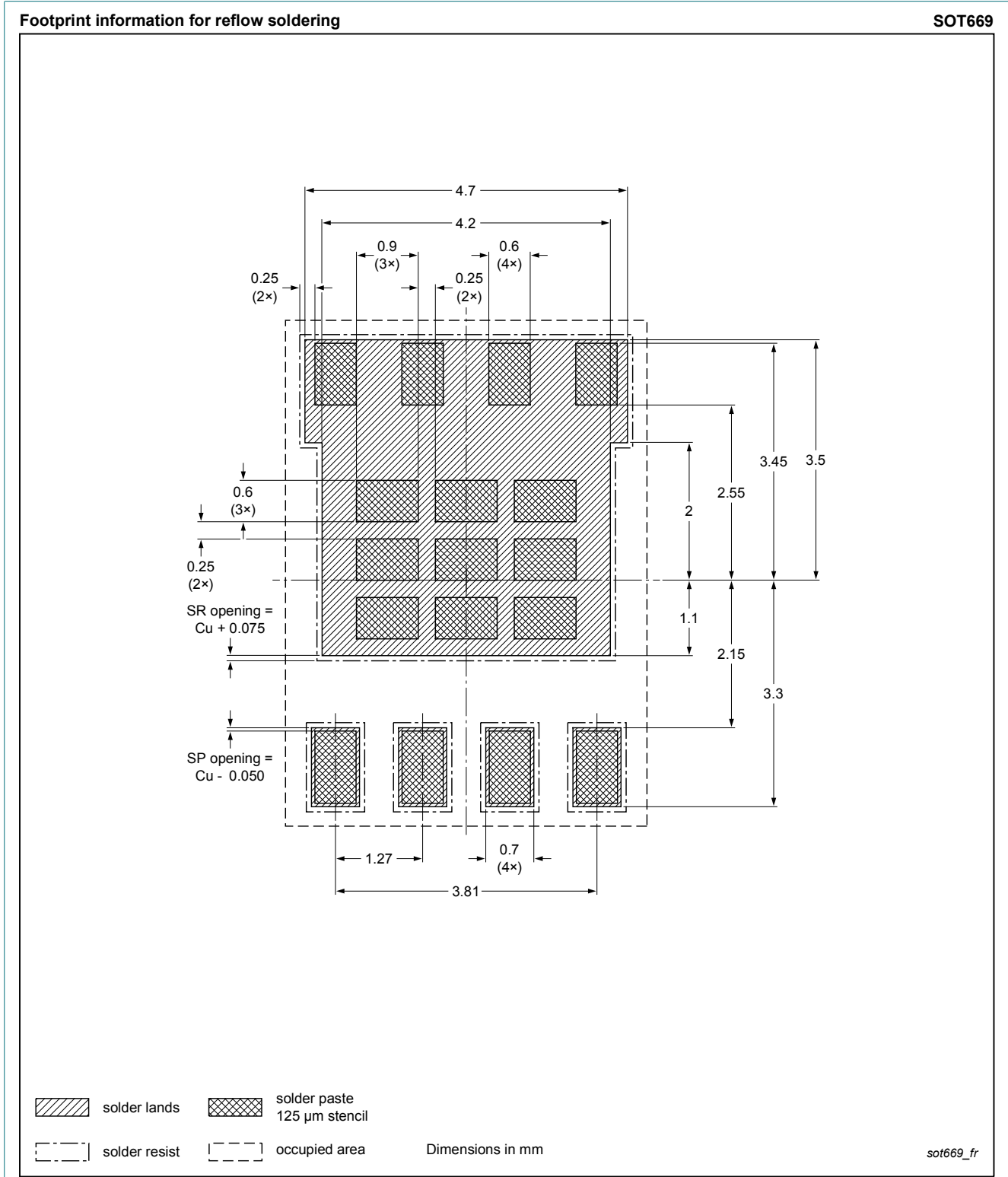
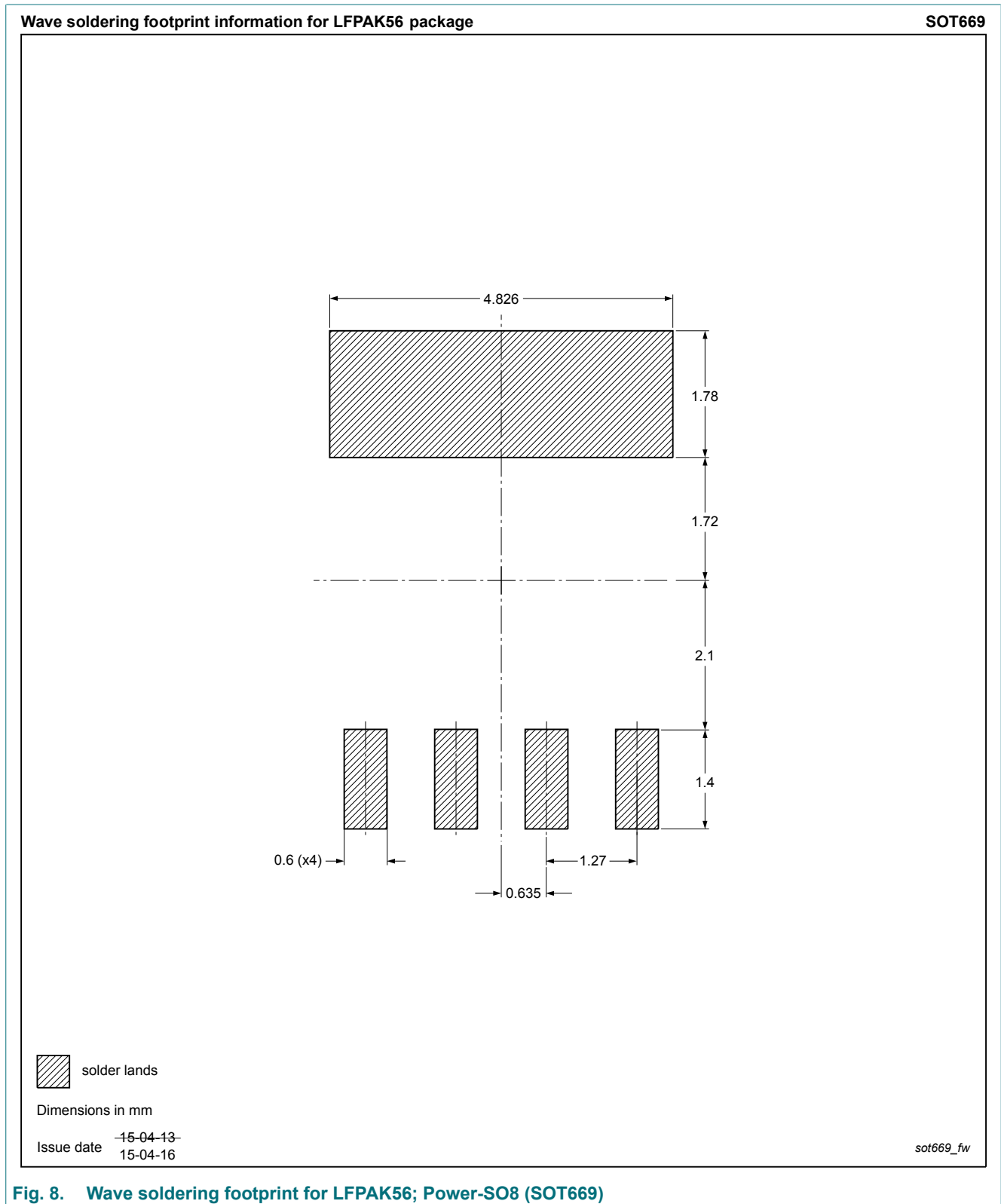


Fig. 7. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)



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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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